PERFORMED ON A VIRTUAL ADDRESS, attorney docket no. RAB 97-001."

IN THE CLAIMS:

Please cancel claims 6 - 37.

Please amend claims 1-5 as follows:

1. (Amended) A circuit for storing physical address translation information to reduce address translation time in a computer system, said circuit comprising:

a) a data path for receiving a virtual address, said virtual address including a segment identifier for identifying a segment [identifier] and a segment offset; and

b) a segment descriptor memory coupled to said data path and selectable by said segment identifier, said memory capable of storing at least the following:

i) linear address information describing the base of the segment,

ii) linear address information describing the limit of the segment, and

iii) a page frame describing at least a portion of a physical address of said segment; and

wherein a tentative memory reference can be initiated based on the virtual address and the information in the segment descriptor memory and without performing a virtual to linear to physical address translation.

2. (Amended) The circuit of claim 1, wherein the information in the segment descriptor memory is stored in one or more registers, and such information can be combined with a portion of the segment offset to create a physical address that is used to initiate the tentative memory reference.

3. (Amended) The circuit of claim 1, wherein the information in the segment descriptor memory is stored in a cache and such information can be combined with a portion of the segment offset to create a physical address that is used to initiate the tentative memory reference.

4. (Amended) The circuit of claim 1, further including a physical address register coupled to the segment descriptor memory for storing a physical address used to initiate the tentative memory reference, said physical address being comprised of the page frame from said segment descriptor memory and a page offset.

a3 Cancel.

5. (Amended) The circuit of claim [4] 1, wherein the [physical address stored in the physical address register is used to perform a memory access] page frame stored in the segment descriptor memory is based on a prior virtual address.

Please add new claims 38 - 81:

a4 Cont.

38. A system for performing address translations, said system generating an actual physical address from a virtual address in a time period T, by calculating a linear address based on said virtual address, and by calculating said actual physical address based on said calculated linear address, said system further including:

a fast physical address generator for generating a fast physical address related to said virtual address in a time < T.

39. The system of claim 38, wherein the fast physical address can be used for generating a memory access faster than a memory access based on said actual physical address.

40. The system of claim 39, including a cancellation circuit for cancelling the memory access if the fast physical address and actual physical address are different.

41. The system of claim 38, wherein the fast physical address is generated based on a combination of physical address information from a different virtual address, and partial linear address information relating to said virtual address.

42. The circuit of claim 38, wherein the fast physical address is generated before said calculated linear address.

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43. A system for performing address translations using a first operation to convert a first virtual address to a first linear address, and a second operation to convert said first linear address to a first physical address, said system further including:

a tentative physical address generator for generating a tentative physical address related to said first virtual address;

wherein the tentative physical address can be generated before said second operation has completed converting said first linear address.

44. The system of claim 43, wherein the tentative physical address can be used for generating a memory access which is faster than a memory access resulting from said first physical address.

45. The system of claim 44, including a cancellation circuit for cancelling the memory access if the tentative physical address and first physical address are different.

46. The system of claim 43, wherein the tentative physical address is generated based on a combination of prior physical address information and partial linear address information relating to said first virtual address.

47. The circuit of claim 43, wherein the tentative physical address is generated before said first operation has completed converting said first virtual address into said first linear address.

48. The circuit of claim 43, wherein said first virtual address is partially converted to a linear address by the fast physical address circuit and is combined with physical address information relating to a prior virtual address to generate the tentative physical address.

49. A system for performing address translations using a first operation to convert virtual addresses to linear addresses, and a second operation to convert said linear addresses to physical addresses, said system further including:

a fast physical address generator for generating fast physical addresses related to said virtual addresses;

wherein the fast physical addresses can be generated while said virtual addresses are being converted in said first operation into said linear addresses.

50. The system of claim 49, wherein the fast physical addresses can be used for generating memory accesses faster than memory accesses resulting from said calculated physical addresses.

51. The system of claim 50, including a cancellation circuit for cancelling the memory accesses if the fast physical addresses and calculated physical addresses are different.

52. The system of claim 49, wherein the fast physical addresses are generated based on a combination of physical address information and partial linear address information relating to said virtual addresses.

53. The system of claim 49, wherein said virtual addresses are partially converted to linear addresses by the fast physical address circuit and are combined with physical address information relating to prior virtual addresses to generate the tentative physical addresses.

54. A system for performing address translations comprising:

a virtual to linear address converter circuit for generating a calculated linear address based on a virtual address; and

a linear to physical address converter circuit for generating a calculated physical address based on the calculated linear address, the calculated physical address including a calculated page frame and a calculated page offset; and

a fast physical address circuit for generating a fast physical address including a fast page frame and a fast page offset;

wherein a memory reference can be generated based on the fast physical address.

55. The system of claim 54, wherein the fast physical address is based on linear address information relating to the virtual address and physical address information relating to a prior virtual address.

56. The system of claim 54, wherein the virtual address is partially converted to a linear address by the fast physical address circuit and is combined with physical address information relating to a prior virtual address to generate the tentative physical address.

57. A system for performing address translations using a first operation to convert a first virtual address to a first linear address, and a second operation to convert said first linear address to a first physical address, the system further including:

an address translation memory, accessible by said system while said first operation is converting said first virtual address, and capable of storing prior physical address information generated during a prior address translation by said second operation based on a prior virtual address;

wherein a fast physical address can be generated based on the prior physical address information and said first linear address before said second operation has completed converting said first linear address.

58. The system of claim 57, wherein the fast physical address can be used for an accelerated memory access which is faster than a memory access resulting from said first physical address.

59. The system of claim 58, including a cancellation circuit for cancelling the fast memory access if the fast physical address and first physical address are different.

60. The system of claim 57, wherein the fast physical address is comprised of:

(iii) a page frame portion based on the prior physical address information; and

(iv) a page offset portion based on the result of converting said first virtual address to a first linear address.

61. A system for performing address translations comprising:

an address translation memory capable of storing:

(i) a portion of a physical address corresponding to a stored page frame; and

(ii) segment base information relating to a virtual address; and

a virtual to linear address converter circuit for generating a calculated linear address based on combining a portion of the virtual address and the segment base; and

a linear to physical address converter circuit for receiving and generating a calculated physical address based on the calculated linear address, the calculated physical address including a first page frame and a first page offset; and

a fast physical address circuit for generating a fast physical address comprised of the stored page frame combined with a fast page offset portion derived from the segment base and the virtual address;

wherein the fast physical address is calculated prior to the generation of said calculated physical address.

62. The system of claim 61, wherein the fast physical address can be used for generating a fast memory access which is generated more quickly than a memory access resulting from said first physical address

63. The system of claim 61, including a cancellation circuit for cancelling the fast memory access if the fast physical address and first physical address are different.

64. The circuit of claim 61, wherein the fast physical address is generated prior to the generation of the first linear address.

65. The system of claim 61, wherein the stored page frame is generated in a prior address translation based on a prior virtual address.

66. A method of performing a translation of a virtual address in a computer system, said method including the steps of :

(a) calculating a fast physical address related to said virtual address; and

(b) calculating a linear address based on said virtual address; and

(c) calculating an actual physical address based on the linear address;

wherein step (a) is completed prior to the completion of step (c), and the fast physical address can be used to initiate a fast memory reference.

67. The method of claim 66, further including a step (d): cancelling the memory access if the fast physical address and actual physical address are different.

68. The method of claim 66, wherein the fast physical address is generated based on a combination of physical address information from a different virtual address, and partial linear address information relating to said virtual address.

69. The method of claim 66, wherein step (a) is completed prior to the completion of step (b).

70. A method of generating memory references based on virtual addresses in a computer system, said method including the steps of:

(a) generating tentative memory references based on said virtual addresses; and

(b) converting said virtual addresses to linear addresses during a segmentation operation; and

(c) converting said linear addresses to physical addresses during a paging operation, so that actual memory references can be made based on said physical addresses;

wherein the tentative memory reference can be generated while said virtual addresses are being converted in said first operation into said linear addresses.

71. The method of claim 70, further including a step (d): cancelling the tentative memory reference if the tentative memory reference and actual memory reference are different.

72. The method of claim 70, wherein the tentative memory reference is generated based on a combination of physical address information and partial linear address information relating to said virtual addresses.

73. The method of claim 70, wherein step (a) is completed prior to the completion of step (b).

74. A method of generating a fast memory reference using a fast physical address derived from a virtual address in a computer system, the method including the steps of:

(a) converting a portion of said virtual address into a partial linear address; and

(b) combining the partial linear address with physical address information obtained from a prior memory reference to generate said fast physical address;

(c) generating a memory reference based on the fast physical address;

(d) converting said virtual address into an actual physical address;

(e) cancelling the memory reference if the fast physical address and actual physical address are different.

75. The method of claim 74, wherein the fast physical address is generated prior to the generation of the linear address.

76. The method of claim 74, wherein the fast physical address is used to generate a fast memory access prior to the generation of the linear address.

77. A method of generating physical addresses from virtual addresses in a computer system, the method including the steps of:

(a) generating a first calculated linear address based on a first virtual address in a first operation; and

(b) generating a fast physical address in a second operation, the fast physical address including linear address information relating to said first virtual address and portions of physical address information relating to said first virtual address; and

(c) generating a first calculated physical address in a third operation based on the first calculated linear address;

wherein the fast physical address is generated prior to the generation of the first calculated physical address.

78. The method of claim 77, wherein the fast physical address is used to generate a tentative memory access prior to the generation of the first calculated physical address.

79. The method of claim 78, including a step (d): cancelling the tentative memory access if the fast physical address and first calculated physical address are different.

80. The method of claim 79, further including a step (e): generating a memory access request based on the first calculated physical address; and (f) storing physical address information relating to the first calculated physical address for use in a later address translation.

81. The method of claim 77, wherein the first and second operations overlap in time, and the fast physical address is generated prior to the generation of the first calculated linear address.